WHAT IS CLAIMED IS:

1. A hardware management apparatus comprising:

at least one semiconductor integrated circuit component which comprises a plurality of semiconductor components, and a first memory for storing first management information used to manage mount states of said plurality of semiconductor components;

at least one circuit board which comprises said at least one semiconductor integrated circuit component, and a second memory for storing second management information used to manage a mount state of said at least one semiconductor integrated circuit component; and

a third memory for storing third management information used to manage a mount state of said at least one circuit board.

2. An apparatus according to claim 1, further comprising:

management information change means for, when the mount states of said plurality of semiconductor components are changed, rewriting the first management information stored in said first memory to indicate changed mount states of said plurality of semiconductor components, for, when the mount state of said at least one semiconductor integrated circuit component is changed, rewriting the second management information stored in said second memory to indicate the changed

mount state of said at least one semiconductor integrated circuit component, and for, when the mount state of said at least one circuit board is changed, rewriting the third management information stored in said third memory to indicate the changed mount state of said at least one circuit board.

3. An apparatus according to claim 1, further comprising an IC card having intellectual property information and a management area for storing fourth management information used to manage the intellectual property information, and

wherein when a management method of the intellectual property information is changed, said management information change means rewrites the fourth management information stored in the management area to indicate the changed management information of the intellectual property information.

4. An apparatus according to claim 1,

wherein the first memory includes a first information area storing information of the plurality of semiconductor components upon manufacture and a second information area storing information of the plurality of semiconductor components after change.

5. An apparatus according to claim 1,

wherein the second memory includes a first information area storing information of the at least one circuit board upon manufacture and a second

information area storing information of the at least one circuit board after change.

6. An apparatus according to claim 1,

wherein the third memory includes a first information area storing information of the at least one circuit board upon manufacture and a second area storing information of the at least one circuit board after change.

7. A hardware management apparatus comprising:

first storage means for storing first management information used to manage a state of hardware upon building a system;

second storage means, provided independently from said first storage means, for storing second management information indicating a current state of the hardware;

management information storage means for, when the state of the hardware is changed after the system was built, storing the second management information indicating the current state of the hardware in said second storage means; and

display means for displaying a changed state of the hardware on the basis of the first management information stored in said first storage means, and the second management information stored in said second storage means.

8. An apparatus according to claim 7,

further comprising an IC card having intellectual

property information and a management area for storing management information used to manage the intellectual property information, and

wherein the display means displays a changed state of the intellectual property information based on the management information stored in the management area.

9. A hardware management apparatus comprising:

a first area storing intellectual property information;

a second area storing management information used to manage the intellectual property information upon manufacture; and

a third area storing management information used to manage the intellectual property information after change,

wherein the intellectual property information stored in the first area is read out under a condition of the management information stored in the second and third areas.

10. An apparatus according to claim 9,

wherein each of the management information stored in the second and third areas includes an access number condition for the intellectual property information.

11. A semiconductor integrated circuit comprising:

a plurality of semiconductor components; and

a memory storing management information used to manage mount state of the plurality of semiconductor

components,

wherein the management information is rewritten, when the mount state of the plurality of semiconductor components changes, to indicate changed mount state of the plurality of semiconductor components.

12. A circuit according to claim 11,

wherein the memory includes a first information area storing information of the plurality of semiconductor components upon manufacture and a second information area storing information of the plurality of semiconductor components after change.

13. A circuit board comprising:

a plurality of semiconductor integrated circuit component; and

a memory storing management information used to manage mount state of the plurality of semiconductor integrated circuits,

wherein the management information is rewritten, when the mount state of the plurality of semiconductor integrated circuits, to indicate changed mount state of the plurality of semiconductor integrated circuits.

14. A circuit board according to claim 13,

wherein the memory includes a first information area storing information of the plurality of semiconductor integrated circuits upon manufacture and a second information area storing information of the plurality of semiconductor integrated circuits after

change.

15. A hardware management method comprising:

storing first management information indicating a state of hardware of a system in a first memory upon building the system;

storing, when the hardware of the system is changed, second management information indicating a changed state of the hardware in a second memory; and

displaying the changed state of the hardware on the basis of the first management information stored in the first memory, and the second management information stored in the second memory.

16. A method according to claim 15, wherein the first and second memories store management information used to manage a mount state of a plurality of semiconductor components of an integrated circuit component.

17. A method according to claim 15, wherein the first and second memories store management information used to manage a mount state of integrated circuit components on a circuit board.

18. A method according to claim 15, wherein the first and second memories store management information used to manage a mount state of circuit boards.